Designing Efficient Online Testable Reversible Adders with New Reversible Gate

Abstract—

Reversible logic is emerging as a promising computing paradigm having its applications in low power VLSI design, quantum computing, nanotechnology and optical computing. In this paper, a new 4\*4 reversible gate termed ‘OTG’ (Online Testable Gate) is proposed suitable for online testability in reversible logic circuits. OTG can also work singly as a reversible full adder with a bare minimum of two garbage outputs. OTG is shown better than the recently proposed R1 gate (introduced for providing online testability in reversible logic circuits), in terms of computation complexity. The proposed reversible gate is combined with the existing 4\*4 Feynman gate to design online testable reversible adders such as ripple carry adder, carry skip adder and BCD adder. The efficient reversible design of two pair rail checker is also shown in this paper. The testable reversible circuits proposed in this work are shown to be better than the recently proposed testable designs in terms of number of reversible gates, garbage outputs and unit delay.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis